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Specifications

1. Title of the Invention

Silicon Single Crystal Having Excellent Oxide Layer Breakdown Voltage Characteristics and Manufacturing Method Thereof

2. Scope of the Patent Claims

(1) A silicon single crystal wafer of at least 100 mm diameter produced by the Czochralski method for which, when oxide layer breakdown voltage of the wafer is evaluated by a voltage ramping method comprising application of polarized direct current to each of numerous MOS diodes to inject a multiplicity of carriers from the silicon substrate in MOS diodes having 5 mm diameter two-layer gate electrodes for which the upper layer of aluminum and the lower layer of doped polysilicon are formed upon the silicon single crystal wafer, oxide layer breakdown voltage of the silicon single crystal is excellent as indicated by at least 60% of the MOS diodes showing a mean electric field of at least 8.0 MV/cm upon application of current at a current density of 1 $\mu A/cm^2$.

(2) A method for production of silicon single crystal of at least 100 mm diameter by the Czochralski method such that the silicon single crystal has excellent oxide layer breakdown voltage characteristics; wherein the crystal growth rate is less than or equal to 0.8 mm/minute.

3. Detailed Explanation of the Invention

(Field of Industrial Use)

The present invention relates to a silicon single crystal and production method thereof by the Czochralski method; wherein the silicon single crystal has excellent oxide layer breakdown voltage characteristics.

(Conventional Technology)

Various types of methods have been known for growth of silicon single crystal. Among such methods, one widely used in industry is the Czochralski method which grows a single crystal ingot by pulling up of a seed crystal contacting a silicon melt within a quartz crucible. Oxide layer breakdown voltage of the single crystal wafer produced by this method (referred to hereinafter as a CZ wafer) is known to be rather low in comparison to a single crystal wafer produced by the floating zone method (referred to hereinafter as an FZ wafer) and a single crystal wafer produced by epitaxial growth upon a CZ single crystal substrate produced by the Czochralski method (referred to hereinafter as an epi wafer) (e.g., page 70 of "Sub-micron Device II, 3 Reliability of the Gate Oxide Layer" by Mitsumasa Koyanagi (published by Maruzen Corp. on Jan. 30th, 1988)). Still the CZ wafer is now widely used as material for devices due to various characteristics. However, in recent years in accompaniment with the increased degree of integration of MOS devices, demands for factory reliability of the gate oxide layer have increased, and oxide layer breakdown voltage is one important material property determining such reliability. Therefore there has come to be a pressing need for development of excellent oxide layer breakdown voltage characteristic type CZ wafers and production technology thereof. However, as can be seen in experimental results of Table 2 obtained by the inventors of the present invention, CZ wafers produced by conventional technology have been unable to attain excellent oxide layer breakdown voltage characteristics.

(Problems to be Solved by the Invention)

As shown in Figure 3, during the Czochralski method, polysilicon is loaded as precursor material into a quartz glass crucible 1. Then this is heated by a heater to form a precursor material melt 2. Thereafter a seed crystal 3 is dipped into precursor material melt 2, and a single crystal ingot 4 is pulled

up while seed crystal 3 and crucible 1 are made to rotate. These operations are normally carried out under an inert gas atmosphere while inert gas flows as indicated by the arrow symbol from a gas feed inlet 6 into a chamber 5. When silicon single crystal is grown by this method, process control factors comprise crucible rotation rate, seed crystal rotation rate, crystal growth atmosphere, melt temperature, crystal pull rate, and other numerous factors. Which of these factors controlled oxide layer breakdown voltage characteristics was previously entirely unknown. Also there has been no report of the capability of manufacturing a CZ wafer showing oxide layer breakdown voltage of the same order as that of an epi wafer, and in fact such a wafer has not existed. For example, a large diameter (50 mm diameter or greater) dislocation-free silicon single crystal grown by the conventional Czochralski method is pulled at a rate of at least 1.2 mm/minute (i.e., see page 64 of "ULSI Process Data Handbook, Chapter 1, Single Crystal Pulling Technology", by Takao Abe, published on April 15th, 1983 by Science Forum Corp.). The CZ wafer produced from silicon single crystal manufactured under such conditions has oxide layer breakdown voltage characteristics (C mode pass rate as explained below) as per the experimental results indicated in Figure 2 that are clearly poor in comparison to the epi wafer.

The objects of the present invention are to provide, for a previously unavailable type of CZ wafer, a silicon single crystal for device manufacturing use having excellent oxide layer breakdown voltage characteristics and to provide control of process conditions so that such silicon single crystal can be produced industrially by the Czochralski method.

(Means to Solve the Problems)

The silicon single crystal of the present invention is a silicon single crystal wafer of at least 100 mm diameter produced by the Czochralski method for which, when oxide layer breakdown voltage of the wafer is evaluated by a voltage ramping method comprising application of polarized direct current to each of numerous MOS diodes to inject a multiplicity of carriers from the silicon substrate in MOS diodes having 5 mm diameter two-layer gate electrodes for which the upper layer of aluminum and the lower layer of doped polysilicon are formed upon the silicon single crystal wafer, oxide layer breakdown voltage of the silicon single crystal is excellent as indicated by at least 60% of the MOS diodes showing a mean electric field of at least 8.0 MV/cm upon application of current at a current density of 1 $\mu A/cm^2$.

Moreover, the method for production of silicon single crystal of the present invention is a method for production of silicon single crystal of at least 100 mm diameter by the Czochralski method such that the silicon single crystal has excellent oxide layer breakdown voltage characteristics; wherein the crystal growth rate is less than or equal to 0.8 mm/minute.

(Operation of the Invention)

Specific operation and composition of the present invention will be explained below while referring to figures.

Figure 1 shows evaluation of oxide layer breakdown voltage of silicon single crystal of the present invention. This is a cross section of a MOS diode formed upon a silicon wafer. A SiO_2 layer 12 is formed upon a silicon wafer 11. Upon this silicon wafer 11 is formed a two-layer gate electrode 15 of 5 mm diameter comprising an aluminum 1 upper layer and a lower layer formed from doped polysilicon 13. Then as shown in Figure 2, numerous MOS diodes 9 having these 5 mm diameter two-layer gate

electrodes 15 are formed upon a silicon wafer 8 (silicon wafer having a SiO_2 layer formed by gate oxidation).

Means to evaluate oxide layer breakdown voltage characteristics of the silicon single crystal of the present invention will be explained using Table 1. A silicon single crystal ingot of at least 100 mm diameter produced by the Czochralski method is processed by the normal industrial manufacturing steps to form a silicon wafer by slicing, lapping, polishing, etc. The obtained wafer is washed (1), gate oxidation is carried out to form a SiO_2 layer (2). A polysilicon layer is deposited (3). Then this polysilicon is doped by ion implantation (6). Oxidation pre-washing (4) and polysilicon oxidation (5) are pre-treatments prior to ion implantation (6). The pre-anneal washing is performed (7). Dry annealing is used to fix dopant within the polysilicon (8). The polysilicon oxide layer is removed by etching (9). An aluminum layer is formed by vaporization-attachment of aluminum (10). Thereafter a positive resist film is applied and patterned during lithography (11) in order to form two-layer gate electrodes of 5 mm diameter. Thereafter the aluminum layer is etched (12), the polysilicon layer is etched (13), and then the resist layer is removed (14). Finally after hydrogen annealing to stabilize the Si/SiO_2 interface (15), a resist layer is applied to the surface to protect the MOS diodes (16), and plasma etching is used to remove the backside polysilicon layer (17). A protective resist layer is again applied to the surface (18), and the backside oxide layer is removed by etching (19). A backside electrode is formed by evaporation-attachment of metal (in the case of p-type) or metal-antimony alloy (in the case of n-type) (20). Finally, after removal of the protective resist layer (21), the voltage ramping method is used to evaluate oxide layer breakdown voltage characteristics (22). The voltage ramping method applies polarized direct current voltage between the aluminum layer 14 and the backside electrode to inject numerous carriers from the silicon substrate while increasing this voltage stepwise over time. For the present invention, the per step voltage increase of this voltage ramping method is 0.25 MV/cm, and the holding time period is 200 ms/step. The proportion (referred to as the C mode pass rate) of individual MOS diodes showing a mean electrical field of at least 8.0 MV/cm in SiO_2 phase 12 when current density through the SiO_2 phase 12 of Figure 1 reaches 1.0 $\mu A/cm^2$ is used to evaluate oxide layer breakdown voltage characteristics of the silicon single crystal. The C mode pass rate of silicon single crystal of the present invention is at least 60%.

Figure 3 is an example of a device for production of silicon single crystal ingot by the Czochralski method that is the object of the present invention. Construction of this device will be explained simply. A chamber 5 is equipped with a gas feed inlet 6 and an exhaust gas port 7. A rotating quartz glass crucible 1 is placed within chamber 5. A pull cable supports a seed crystal 3 at the tip of a (not illustrated) chuck. Using a device such as that shown in Figure 3, as a single crystal ingot 4 is pulled up from precursor material melt 2 contained in crucible 1, and as a silicon single crystal is grown at the solid-melt interface, the present invention sets the crystal pull rate at 0.8 mm/minute or less. When the pull rate is higher than this value, the C mode pass rate is less than 60% and becomes equivalent to that of conventional silicon single crystal. However, when the pull rate is 0.8 mm/minute or less, C mode pass rate improves to 60% or greater. Furthermore, when the pull rate is 0.5 mm/minute or less, the C mode pass rate becomes 90% or better which is nearly equivalent to that of an epi wafer, and gate oxide layer reliability markedly improves.

[Working Examples]

Working examples of the present invention will next be explained.

The device shown in Figure 3 was used. The quantity of precursor material melt 2 prior to pulling was 35 to 65 kg. Argon as the inert gas was fed at 50 to 100 NL/minute, and single crystal ingot 4 was pulled at a rate of 0.8 mm/minute or less to grow single crystal. For comparison with the silicon single crystal of the present invention, single crystal ingot was also produced by pulling at a rate exceeding 0.8 mm/minute. Manufacturing conditions and characteristics of the obtained silicon single crystal wafers are shown in Table 2. Here sample no. 5 is a single crystal ingot pulled at a rate of 0.4 mm/minute during continuous feeding of precursor material polysilicon into melt 2. Moreover, sample no. 9 and 10 are single crystal ingots pulled while a magnetic field is applied. From these single crystal ingots, wafers were sliced, lapped, and polished, etc. to produce silicon wafers by the typically used industrial steps. Single-sided mirror-surface CZ wafers were produced.

Oxide layer breakdown voltage characteristics of these CZ wafers were determined as the C mode pass rate by the steps of Table 1 as explained previously to evaluate these CZ wafers. As made clear by the results shown in Table 2, CZ wafer oxide layer breakdown voltage characteristics were markedly improved to a previously unimaginable high level by setting the crystal pull rate to 0.8 mm/minute or less.

Table 1

No.	Step	Conditions
1	wafer wash	60 seconds immersion in 1.5 wt% HF, followed by ultrapure water rinse
2	gate oxidation	high temperature oxidation at 1000°C in dry oxygen to form about 250 Å thick oxide layer (layer thickness measurement by addition)
3	polysilicon layer deposition	640°C deposition temperature, non-doped polysilicon layer, 5000 Å thick
4	pre-oxidation wash	5 minutes immersion at 1000°C in 97% H_2SO_4 and H_2O_2 (3:1 volume ratio), followed by rinse in ultrapure water, followed by immersion for 60 seconds in 1.5 wt% HF, followed by rinse in ultrapure water [*TRANSLATOR'S NOTE: 1000°C looks like an error in the source text.*]
5	polysilicon oxidation	high temperature oxidation at 900°C in dry oxygen to form about 300 Å thick oxide layer (layer thickness measurement by addition)
6	ion implantation	n-type : doped at 5×10^{15} cm^{-2}, acceleration voltage of 30 - 35 keV; p-type : doped at 10^{16} cm^{-2}, acceleration voltage of 80 keV
7	pre-anneal wash	5 minutes immersion at 100°C in 97% H_2SO_4 and H_2O_2 (3:1 volume ratio), followed by rinse in ultrapure water, followed by immersion for 60 seconds in 1.5 wt% HF, followed by rinse in ultrapure water
8	dry anneal	30 minutes in nitrogen at 900°C
9	polysilicon layer etching	in mixture of 40% NH_4F : 50% HF at 10 : 1 volume ratio
10	Al evaporation-attachment	resistance heating evaporation-attachment, 2000 - 5000 Å
11	lithography	positive resist, 1 μm thick
12	Al etching	in mixture of 85% H_3PO_4 : 70% HNO_3 at 19 : 1 volume ratio
13	polysilicon etching	reactive plasma etching, CF_4
14	resist removal	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
15	hydrogen anneal	in H_2 (2×10^3 cc/minute) + N_2 (10×10^3 cc/minute) at 400°C for 30 minutes
16	resist application	2 μm resist thickness
17	backside polysilicon etching	reactive plasma etching, CF_4
18	resist application	2 μm resist thickness
19	backside oxide etching	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
20	backside electrode evaporation-attachment	electron bombardment heating, about 2000 Å thickness, p-type = Au, n-type = AuSb
21	resist removal	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
22	evaluation of oxide layer breakdown voltage characteristics	voltage ramping method

Table 2

Sample No.	Crystal pull rate (mm/ min.)	C mode pass rate (%)	Resistivity (Ω cm)	Oxygen conc. [10^{17}/cm^{-3}]	Carbon conc [10^{17}/cm^{-3}]	Type	Orientation	Class	Comments
1	0.4	94-100	6.08	7.23	< 1.00	P	(100) K	H	
2	0.4	94-100	8.21	8.66	3.72	P	(100)	H	
3	0.4	94-100	10.45	9.81	5.66	P	(100)	H	
4	0.4	94-100	11.37	10.74	< 1.00	P	(100)	H	
5	0.4	94-100	15.74	11.74	< 1.00	P	(100)	H	cont. Si feed
6	0.5	93-100	12.33	9.25	10.44	P	(100)	H	
7	0.5	93-100	3.54	9.88	< 1.00	N	(100)	H	
8	0.5	93-100	1.01	8.25	< 1.00	P	(100)	H	
9	0.4	94-100	8.89	3.21	2.94	N	(100)	H	MCZ
10	0.4	94-100	9.44	4.74	< 1.00	P	(100)	H	MCZ
11	0.4	93-95	8.86	9.29	< 1.00	P	(111) K	H	
12	0.4	93-99	10.96	8.67	< 1.00	N	(111) K	H	
13	0.6	85-94	12.71	10.38	4.11	P	(100)	H	
14	0.7	73-88	8.52	9.99	< 1.00	P	(100)	H	
15	0.8	60-84	6.44	7.85	1.19	P	(100)	H	
16	0.9	35-65	11.33	11.62	< 1.00	P	(100)	R	
17	1.1	12-44	10.45	9.99	< 1.00	N	(100) K	R	
18	1.5	8-28	10.87	10.42	1.23	P	(100)	R	
19	--	93-100	15.35	--	--	P	(100)	R	epi wafer
20	2.0	7-25	8.26	10.44	< 1.00	P	(100)	R	

[TRANSLATOR'S NOTE: "[10^{17}/cm^{-3}]" looks like an error in the source text.]

H = working example of the present invention; R = comparative example; K = 4° tilt angle; P = p-type; N = n-type.

[Results of the Invention]

As explained previously, the present invention is applicable to wafers used for MOS devices due the increased reliability of the gate oxide layer due to excellent oxide layer breakdown voltage characteristics not hitherto obtained for CZ wafer.

4. Simple Explanation of the Figures

Figure 1 is a cross-sectional drawing of part of a MOS diode formed upon a silicon wafer for evaluation of oxide layer breakdown voltage characteristics of silicon single crystal of the present invention. Figure 2 is a cross-sectional drawing of a MOS diode formed upon this wafer. Figure 3 is a drawing showing construction of one example of a device used for production by the Czochralski method.

1 .... quartz glass crucible
2 .... precursor material melt
3 .... seed crystal
4 .... silicon single crystal ingot
5 .... chamber

6 .... gas feed inlet
7 .... exhaust gas port
8 .... silicon wafer that has a SiO_2 layer formed by gate oxidation
9 .... MOS diode (5 mm electrode diameter)
10 .... MOS diode (1, 2, 3, 4, and 6 mm electrode diameter)
11 .... silicon substrate
12 .... SiO_2 layer (roughly 250 Å thick)
13 .... polysilicon layer (roughly 5000 Å thick)
14 .... aluminum layer (roughly 2000 - 5000 Å thick)
15 .... two-layer gate electrode

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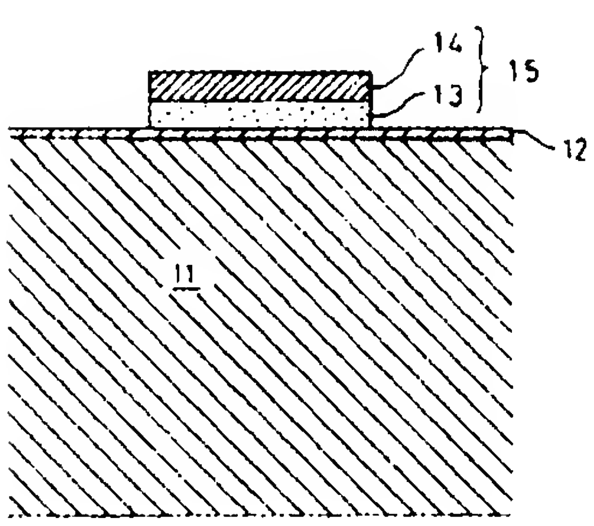
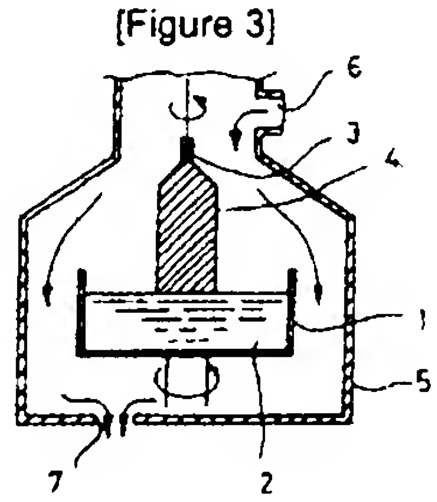
Applicant: Nittetsu Electron Corporation

Agent: Mikio HATTA, Attorney (and one other person)

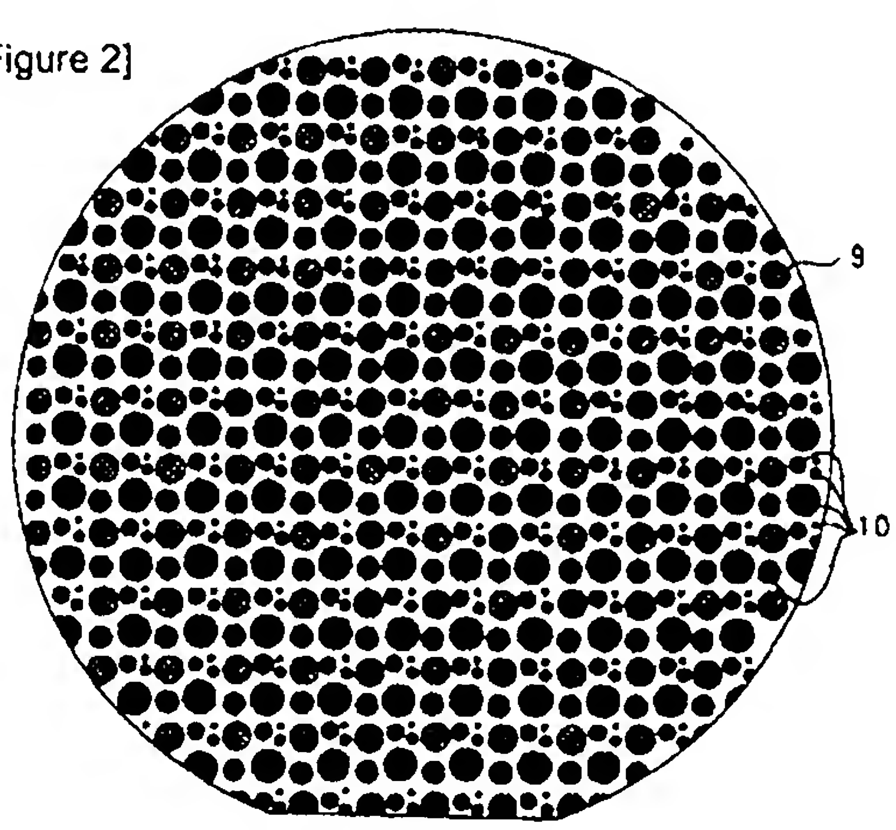
[Figure 1]



[Figure 3]



[Figure 2]



Amendment of Proceedings (formal)

July 28th, 1989

Commissioner of the Patent Office, Mr. Bungi Yoshida

1. Case Identification

   Patent Filing No. Hei 1-086505

2. Title of the Invention

   Silicon Single Crystal Having Excellent Oxide Layer Breakdown Voltage Characteristics and Manufacturing Method Thereof

3. Amending Party

Relationship to the case:	Patent Applicant
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5. Date of Amendment Order

   Self-originated amendment

6. Object of Amendment

   (1) Column of names of the "inventor" of the application document

   (2) Column titled "Detailed Description of the Invention" of the specifications document

   (3) Figure 2

7. Contents of the Amendment

(1) An inventor's name is corrected as per the attached correction request.

(2) The specifications document is amended as explained below.

(a) Before "epi wafer" of the first line of page 3, insert "abbreviated as".

(b) Change "factory reliability" mentioned in line 9 of page 3 to read "improved reliability".

(c) Change "Figure 2" mentioned in line 2 of page 5 to read "Table 2".

(d) Change "aluminum 1" mentioned in line 19 of page 6 to read "aluminum 14".

(e) Change "SiO_2 phase" mentioned both in line 5 and line 7 of page 9 to each read "SiO_2 layer".

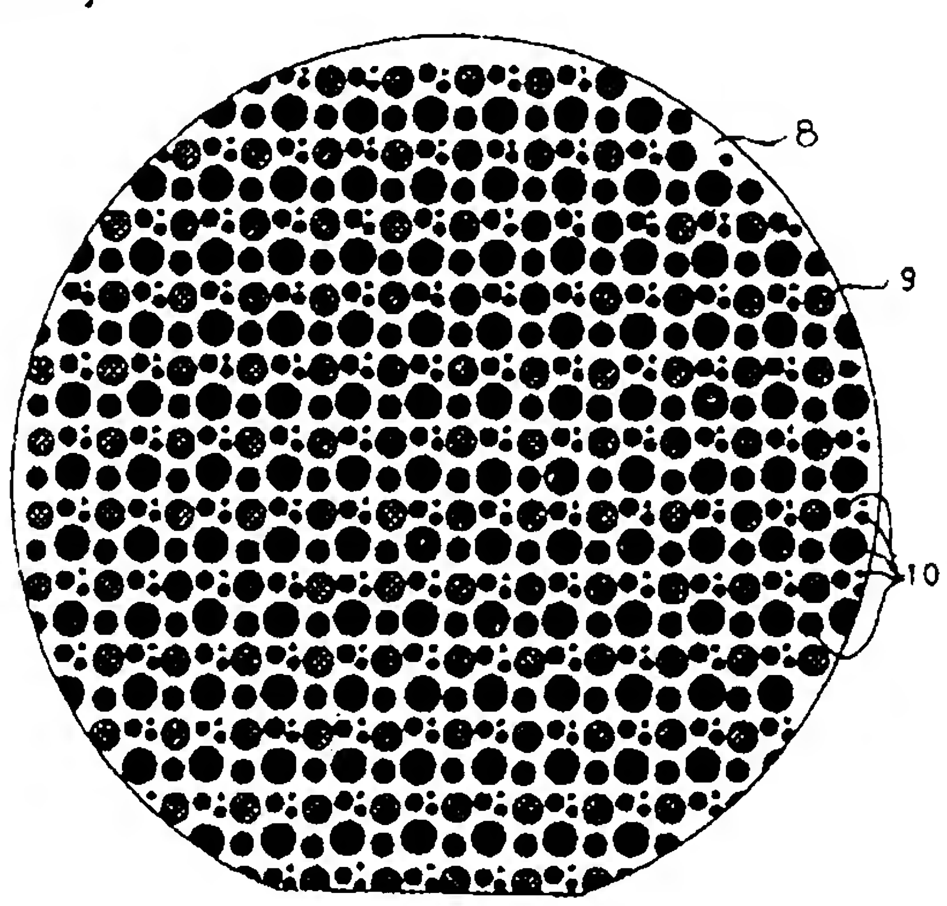
(f) Correct the spelling of "pull rate" in line 14 of page 11.

(3) As per the attachment, add the identification number 8 and referencing line to Figure 2.

8. List of Attached Documents

(1) Grounds for Rectification Document	1
(2) Proof of Registration-Non-registration	1
(3) Proof of Assignment	1 each
(4) Approval	1 each

[Figure 2]



Job Name:

...8 Jap. Pat. - Eng. Trans..PDF

Job Owner Name:

.TFM.Senniger

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Morita Patent

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Inventor: Etsuro Morita, Mikio Kishimoto, Jiro Ryuta, Yasushi Shimanuki, Toshiro Tanaka

Field of the Invention

Claim 1

Silicon wafers that do not have etch pits on the surface. These wafers are processed from silicon single crystal manufactured by the Czochralski method.

Summary of the Invention

Application of the Invention

This invention is applied for silicon wafers that are used for manufacturing LSI, for the detail, this invention is provided for an improvement of silicon wafers, which are processed from silicon single crystal manufactured by Czochralski method.

Conventional Technology

Conventional Czochralski method silicon wafers were processed from slicing pulled single crystal silicon by slicing machine. These sliced silicon wafers are lapped or ground, furthermore, chemical etching is taken place for the wafers to remove mechanical damage from processing.

And then, these silicon wafers are polished on the surface and cleaned as final processes.

The Issue(s) to be solved by this Invention

However, either high density small defect or low density large defect exists on such conventional Czochralski method silicon wafers. These defects appear on the wafer surface as etch pits by ammonia-based cleaning after polishing.

An electrical characteristic of the silicon wafers is damaged by the defects mentioned

above.

And. as a result. yield is low at the manufacturing of the silicon wafers.

Accordingly. an object of this invention is to provide silicon wafers that have improved electrical characteristic and high yield at their manufacturing.

The Method to Solve Issue(s)

This invention is to provide silicon wafers that do not have etch pits on the surface. which are processed from silicon single crystals pulled by using Czochralski method.

Effects

Regarding the silicon wafers from this invention. no etch pits practically exist on the wafer surface after ammonia-based cleaning after polishing. That is. no defects mentioned above exit near the silicon wafer surface from this invention.

To produce such no etch pits wafers, single crystal silicon pulled by Czochralski method needs to be cooled down at certain cooling rate. For example, during the total cooling period from 1200°C to 800°C of the single crystal silicon, the cooling rate is controlled less than 0.4°C/minite.

As a result, wafers that contains no etch pits, which means no defects, are obtained. Therefore. the electrical characteristic of the wafers is improved and manufacturing yield also improved by this invention.

Example

We explain examples of this invention.

A Czochralski method is used to grow silicon single crystal for this invention.

In this case, total cooling rate from 1200 °C to 800°C during cooling period of the pulling crystal is controlled to less than 0.4°C/minute. The cooling rate can be 0.5°C/minute-1.0°C/minute.

The crystal is processed pulled by method described above to polished wafers by using conventional wafering processes.

The wafers from above, which is P type <100> orientation, are cleaned for 20 minutes at 85°C, which is higher temperature than normal process to enhance its etching ability, by using ammonia-based cleaning solution such as $NH_4OH/H_2O_2/H_2O$ (1:1:5).

The cleaning is repeated 10 times. As a result, the etch pits that are 0.1 μm in the size can be counted by a particle counter, which is common in the art.

From above result, no formation of etch pits in the size of 0.2 μm that is the customer requirement to-date are observed on the wafer surface.

For example, when a particle counter, which is common in the art, counts particles, 1,000 of etch pits are observed on silicon wafers from conventional Czochralski method after 10 times repeated cleaning by using ammonia-based cleaning solution. On the other hand, particles are 0, that is, no etch pits are observed on the wafers from this invention when same particle counter is used